

LM715 High Speed Operational Amplifier

General Description

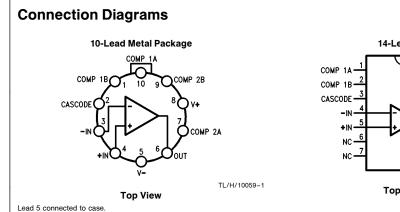
The LM715 is a high speed, high gain, monolithic operational amplifier intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The LM715 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages.

Features

- High slew rate— 100 V/μs (Inverting, A_V = 1) typically
- Fast settling time— 800 ns typically
- Wide bandwidth— 65 MHz typically
- Wide operating supply range
- Wide input voltage ranges

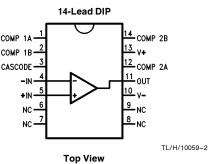
Applications

- Video amplifiers
- Active filters
- High speed data conversion



Ordering Information

Device Code	Package Code	Package Description		
LM715MH	H10C	Metal		
LM715CH	H10C	Metal		
LM715MJ	J14A	Ceramic DIP		
LM715CJ	J14A	Ceramic DIP		



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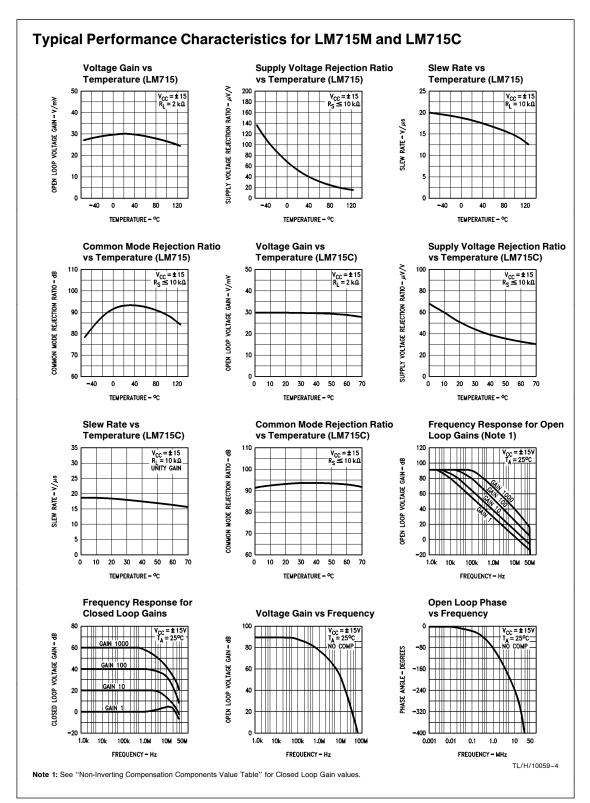
October 1989

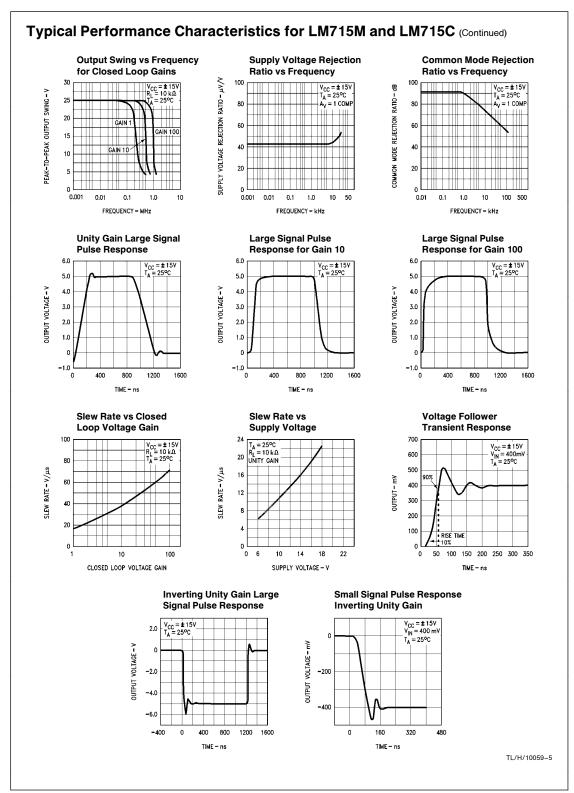
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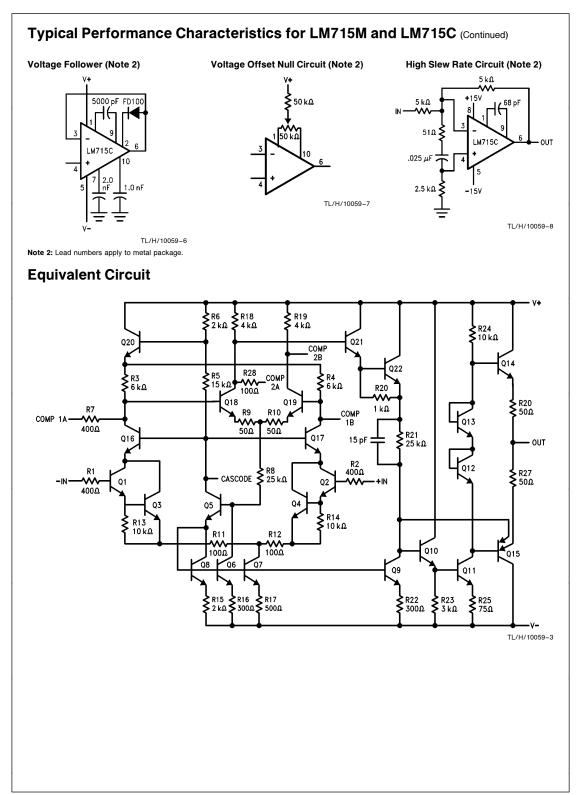
RRD-B30M115/Printed in U. S. A.

please	contact the	National Se	vices are requ miconductor S nd specification	ales	10	nal Pow L-Metal L-Cerar	Can	ipation (Notes 1,	2)		1.07W 1.36W
Storage	Temperature Ra	ange	-65°C to +1	75°C	Supp	oly Volta	ige					±18\
Commercial (LM715C)			−55°C to +1 0°C to +		Differential Input Voltage Input Voltage (Note 3)						±5\ ±15\	
Metal	mperature Can and Ceram ring, 60 sec.)	nic DIP	3	00°C								
	5M and L rical Char		CS T _A = 25°C,	$V_{CC} = \pm$: 15V, ur	nless otl	nerwise	specifie	d			
Symbol	Para	meter	Con	ditions	F		_M715N	1		LM7150		Uni
-						Min	Тур	Max	Min	Тур	Max	<u> </u>
V _{IO}	Input Offset V		$R_{S} \le 10 \text{ k}\Omega$				2.0	5.0		2.0	7.5	m\
10	Input Offset C						70	250		70	250	n/
IB 7	Input Bias Cur						400	750		400	1500	n/
<u>z</u>	Input Impedar						1.0			1.0		M
RO OF	Output Resist Supply Currer						75 5.5	7.0		75 5.5	10	m.
<u>cc</u> 2	Power Consul						165	210		165	300	m
c / _{IR}	Input Voltage	1				±10	±12	210	±10	±12	300	
Avs	Large Signal \	-	R _L ≥ 2.0 kΩ	$V_{0} = $	+ 10V	15	30		10	30		V/r
/	Settling Time	ronage dann	$V_0 = \pm 5.0$	-		10	800		10	800		n
TR	Transient	Rise Time	$V_{\rm I} = 400 {\rm m}$	-			30	60		30	75	n
	Response Overshoot			· , · · v			25	40		25	50	%
SR	Slew Rate		A _V = 100				70			70		-
			$A_{V} = 10$				38			38		V/μs
			$A_V = 1.0$ (N	Ion-Inver	ting)	15	18		10	18		1 V/
			$A_V = 1.0$ (Ir	nverting)			100			100		
The follo LM715C	wing specificati	ons apply ove	r the range of -5	55°C ≤ T	A ≤ +1	125°C fo	or the LN	M715M,	and 0°C	≤ T _A ≤	+70°C	for th
Symbol	Paran	neter	Conditions		LM715	-			LM715			Uni
			D	Min	Тур	Max	-	Min	Тур		Max	
V _{IO}	Input Offset	-	$R_{S} \le 10 k\Omega$			7.5	_				10	m
10	Input Offset	Current	$T_A = T_A Max$			250 800					250 750	nA
I _{IB}	Input Bias Ci	irrent	$T_{A} = T_{A \text{ Min}}$ $T_{A} = T_{A \text{ Max}}$			0.75					1.5	
ιB	input bias of		$T_A = T_A Max$			4.0					7.5	μΑ
CMR	Common Mo Rejection	de	$R_{S} \le 10 \text{ k}\Omega$	74	92			74 ote 4)	92 (Note 4	4)	110	dE
PSRR	Power Suppl Rejection Ra	atio	$R_{S} \leq 10 \ k\Omega$		45	300)		45 (Note 4		400 ote 4)	μV
A _{VS}	Large Signal Voltage Gair	ı	$\begin{array}{l} R_L \geq 2.0 \ k\Omega, \\ V_O = \ \pm 10 V \end{array}$	10		_		8				V/n
VOP	Output Volta	ae Swina	$R_L = 2.0 k\Omega$	±10	±13			±10	±13			V

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, and the 14L-Ceramic DIP at 9.1 mW/°C. **Note 3:** For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage. **Note 4:** $T_A = 25^{\circ}C$ only.







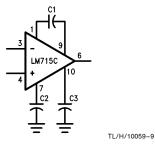
Applications Information

Non-Inverting Compensation Components Values

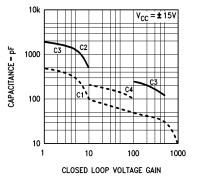
Closed Loop Gain	C1	C2	C3					
1000	10 pF							
100	50 pF		250 pF					
10 (Note)	100 pF	500 pF	1000 pF					
1	500 pF	2000 pF	1000 pF					

Note: For gain 10, compensation may be simplified by removing C2, C3 and adding a 200 pF capacitor (C4) between Lead 7 and 10.

Frequency Compensation Circuit



Suggested Values of Compensation Capacitors vs Closed Loop Voltage Gain



TL/H/10059-10

Layout Instructions

Layout—The layout should be such that stray capacitance is minimal.

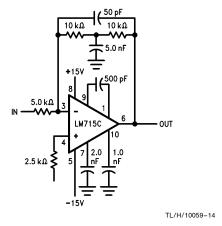
Supplies—The supplies should be adequately bypassed. Used of 0.1 μF high quality ceramic capacitors is recommended.

Note: All lead numbers on this page apply to metal package.

Ringing—Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100Ω . Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

Latch Up—This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between leads 6 and 2 with the cathode toward lead 2 is the recommended preventive measure.

Typical Applications



High Speed Integrator

