National Semiconductor

August 2000

# LM6118/LM6218 Fast Settling Dual Operational Amplifiers

## General Description

The LM6118/LM6218 are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

## Features

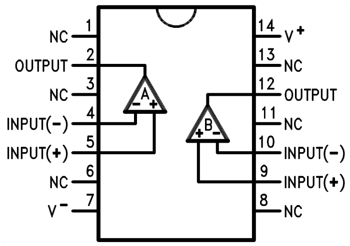
| | **Typical** |
|---|---|
| ■ Low offset voltage: | 0.2 mV |
| ■ 0.01% settling time: | 400 ns |
| ■ Slew rate $A_v = -1$: | 140 V/µs |
| ■ Slew rate $A_v = +1$: | 75 V/µs |
| ■ Gain bandwidth: | 17 MHz |
| ■ Total supply current: | 5.5 mA |
| ■ Output drives 50Ω load (±1V) | |

## Applications

- D/A converters
- Fast integrators
- Active filters

## Connection Diagrams and Order Information

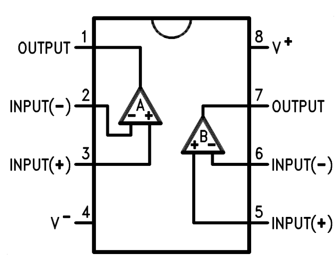
**Small Outline Package (WM)**




DS010254-3

**Top View**
**Order Number LM6218WM, LM6218WMX**
**See NS Package Number M14B**

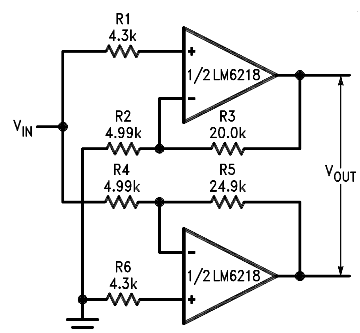
**Dual-In-Line Package (J or N)**




DS010254-4

**Top View**
**Order Number LM6118J/883 or LM6218N**
**See NS Package Number N08E, J08A**

## Typical Applications




DS010254-1

Single ended input to differential output
$A_V = 10$, BW = 3.2 MHz
40 $V_{PP}$ Response = 1.4 MHz
$V_S = \pm 15V$

**Wide-Band, Fast-Settling**
**40 $V_{PP}$ Amplifier**

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Total Supply Voltage | 42V |
| Input Voltage | (Note 2) |
| Differential Input Current (Note 3) | ±10 mA |
| Output Current (Note 4) | Internally Limited |
| Power Dissipation (Note 5) | 500 mW |
| ESD Tolerance | |
| (C = 100 pF, R = 1.5 kΩ) | ±2 kV |
| Junction Temperature | 150˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Temperature | |
| (Soldering, 10 sec.) | 300˚C |

## Operating Temp. Range

| | |
|---|---|
| LM6118 | −55˚C to +125˚C |
| LM6218 | −40˚C to +85˚C |

## Electrical Characteristics

±5V ≤ $V_S$ ≤ ±20V, $V_{CM}$ = 0V, $V_{OUT}$ = 0V, $I_{OUT}$ = 0A, unless otherwise specified. Limits with standard type face are for $T_J$ = 25˚C, and **Bold Face Type** are for **Temperature Extremes.**

| Parameter | Conditions | | Typ 25˚C | LM6118 Limits (Note 6) | LM6218 Limits (Note 6) | Units |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_S$ = ±15V | | 0.2 | 1<br>**2** | 3<br>**4** | mV (max) |
| Input Offset Voltage | V− + 3V ≤ $V_{CM}$ ≤ V+ − 3.5V | | 0.3 | 1.5<br>**2.5** | 3.5<br>**4.5** | mV (max) |
| Input Offset Current | V− + 3V ≤ $V_{CM}$ ≤ V+ − 3.5V | | 20 | 50<br>**250** | 100<br>**200** | nA (max) |
| Input Bias Current | V− + 3V ≤ $V_{CM}$ ≤ V+ − 3.5V | | 200 | 350<br>**950** | 500<br>**1250** | nA (max) |
| Input Common Mode Rejection Ratio | V− + 3V ≤ $V_{CM}$ ≤ V+ − 3.5V<br>$V_S$ = ±20V | | 100 | 90<br>**85** | 80<br>**75** | dB (min) |
| Positive Power Supply Rejection Ratio | V− = −15V<br>5V ≤ V+ ≤ 20V | | 100 | 90<br>**85** | 80<br>**75** | dB (min) |
| Negative Power Supply Rejection Ratio | V+ = 15V<br>−20V ≤ V− ≤ −5V | | 100 | 90<br>**85** | 80<br>**75** | dB (min) |
| Large Signal Voltage Gain | $V_{out}$ = ±15V<br>$V_S$ = ±20V | $R_L$ = 10k | 500 | 150<br>**100** | 100<br>**70** | V/mV (min) |
| | $V_{out}$ = ±10V<br>$V_S$ = ±15V | $R_L$ = 500<br>(±20 mA) | 200 | 50<br>**30** | 40<br>**25** | V/mV (min) |
| $V_O$ Output Voltage Swing | Supply = ±20V | $R_L$ = 10k | 17.3 | ±17 | ±17 | V (min) |
| Total Supply Current | $V_S$ = ±15V | | 5.5 | 7<br>**7.5** | 7<br>**7.5** | mA (max) |
| Output Current Limit | $V_S$ = ±15V, Pulsed | | 65 | 100 | 100 | mA (max) |
| Slew Rate, Av = −1 | $V_S$ = ±15V, $V_{out}$ = ±10V<br>$R_S$ = $R_f$ = 2k, $C_f$ = 10 pF | | 140 | 100<br>**50** | 100<br>**50** | V/µs (min) |
| Slew Rate, Av = +1 | $V_S$ = ±15V, $V_{out}$ = ±10V<br>$R_S$ = $R_f$ = 2k, $C_f$ = 10 pF | | 75 | 50<br>**30** | 50<br>**30** | V/µs (min) |
| Gain-Bandwidth Product | $V_S$ = ±15V, $f_o$ = 200 kHz | | 17 | 14 | 13 | MHz (min) |
| 0.01% Settling Time<br>$A_V$ = −1 | $\Delta V_{out}$ = 10V, $V_S$ = ±15V,<br>$R_S$ = $R_f$ = 2k, $C_f$ = 10 pF | | 400 | | | ns |
| Input Capacitance | Inverter | | 5 | | | pF |
| | Follower | | 3 | | | pF |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

**Note 2:** Input voltage range is ($V^+$ − 1V) to ($V^-$).

**Note 3:** The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

## Electrical Characteristics (Continued)

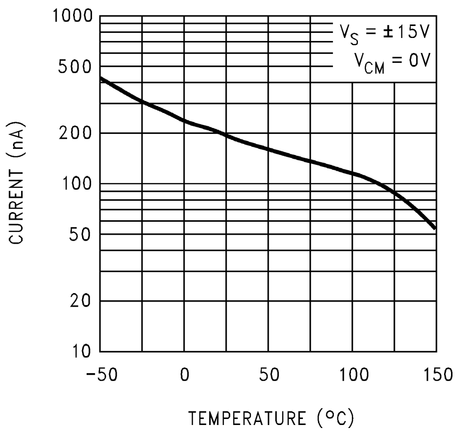
**Note 4:** Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

**Note 5:** Devices must be derated using a thermal resistance of 90˚C/W for the N and WM packages.

**Note 6:** Limits are guaranteed by testing or correlation.

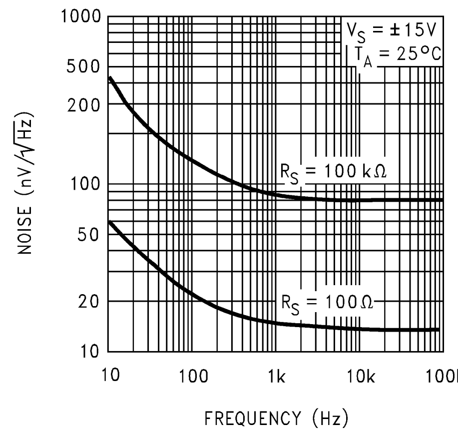
## Typical Performance Characteristics

### Input Bias Current



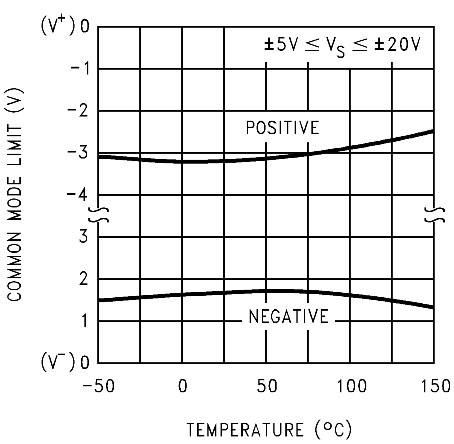

DS010254-25

### Input Noise Voltage



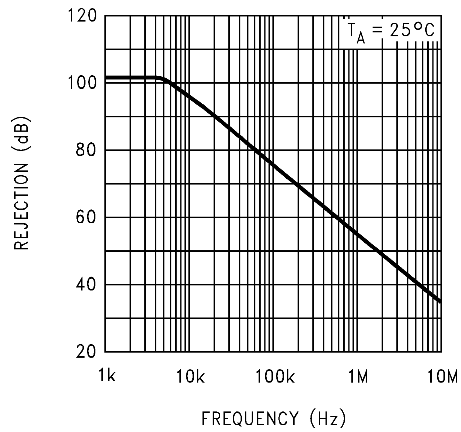

DS010254-26

### Common Mode Limits



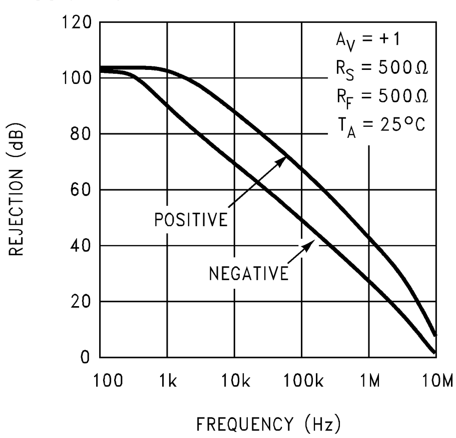

DS010254-27

### Common Mode Rejection



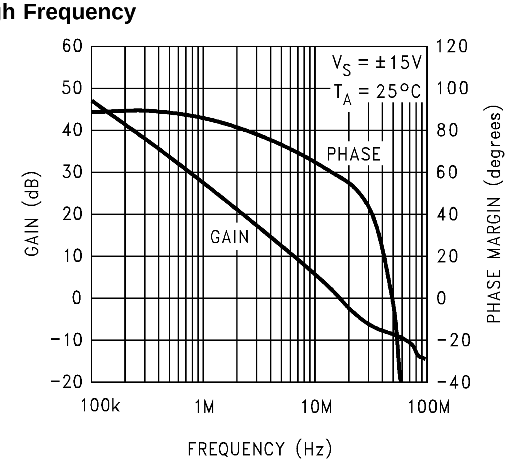

DS010254-28

### Power Supply Rejection




DS010254-29

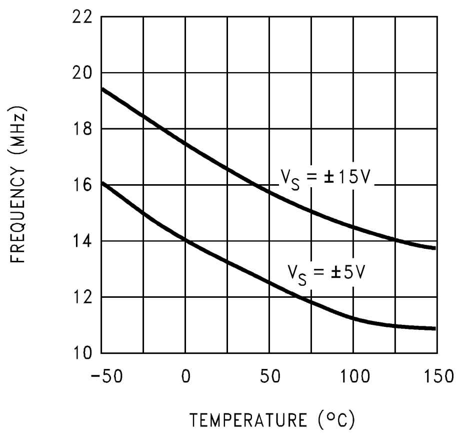
### Frequency Response High Frequency




DS010254-30

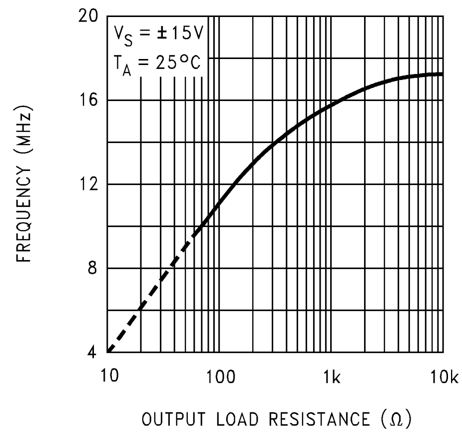
## Typical Performance Characteristics (Continued)

### Unity Gain Bandwidth



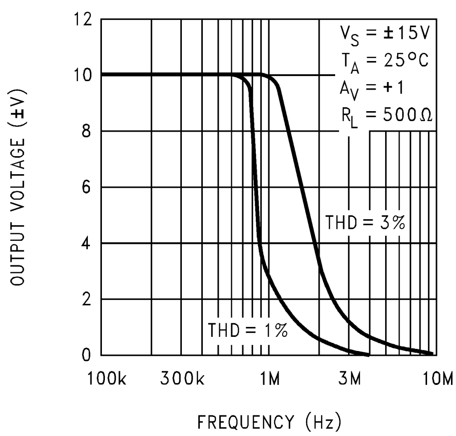

DS010254-31

### Unity Gain Bandwidth vs Output Load



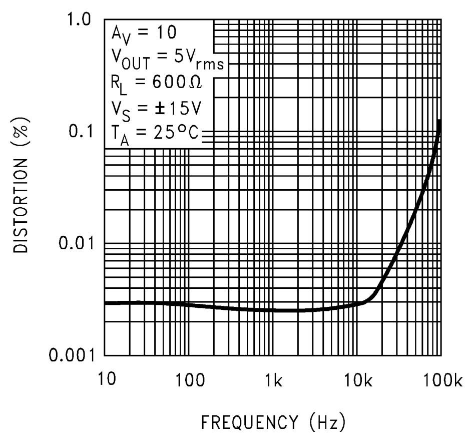

DS010254-32

### Large Signal Response (Sine Wave)



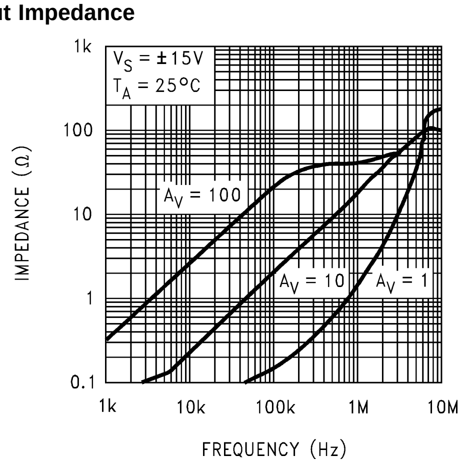

DS010254-33

### Total Harmonic Distortion



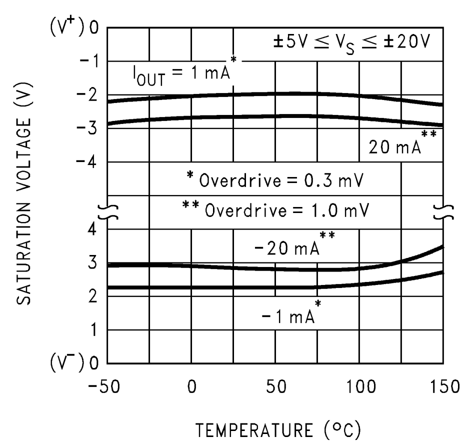

DS010254-34

### Output Impedance




DS010254-35

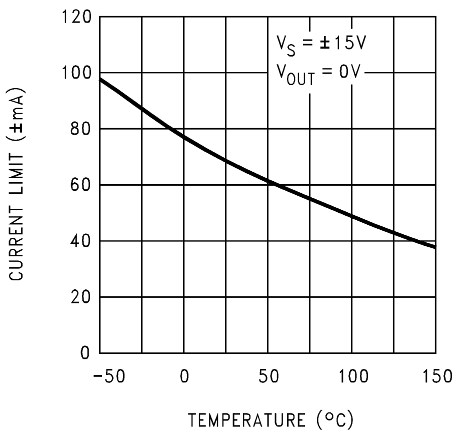
### Output Saturation




DS010254-36

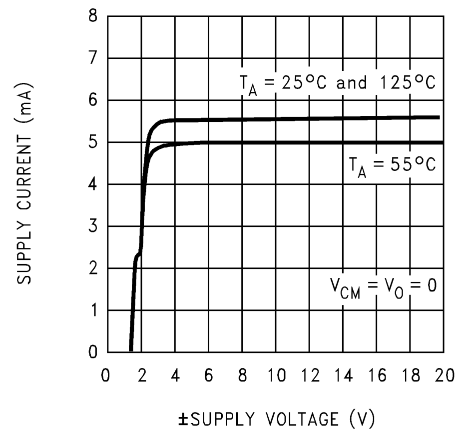
## Typical Performance Characteristics (Continued)

### Output Current Limit



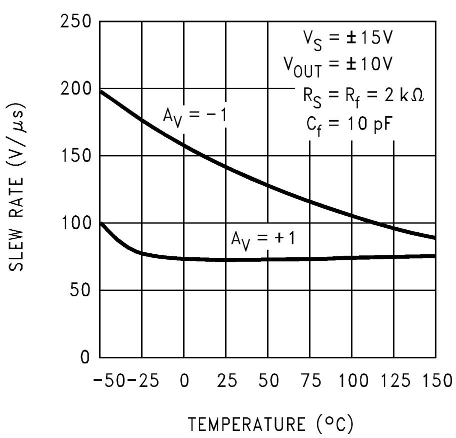

DS010254-37

### Supply Current (Both Amplifiers)



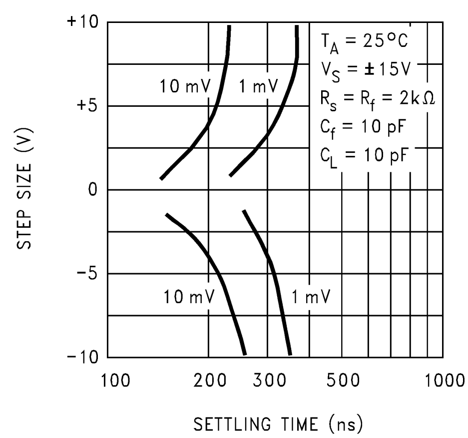

DS010254-38

### Slew Rate



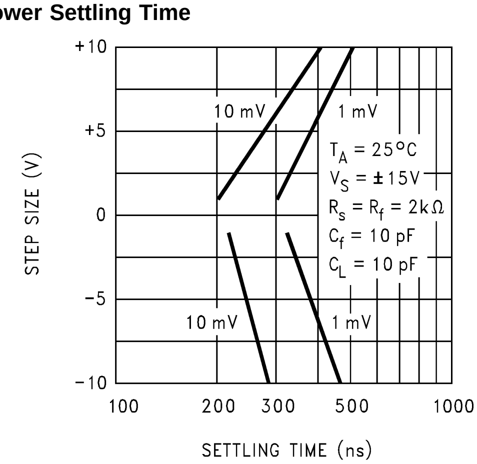

DS010254-39

### Inverter Settling Time



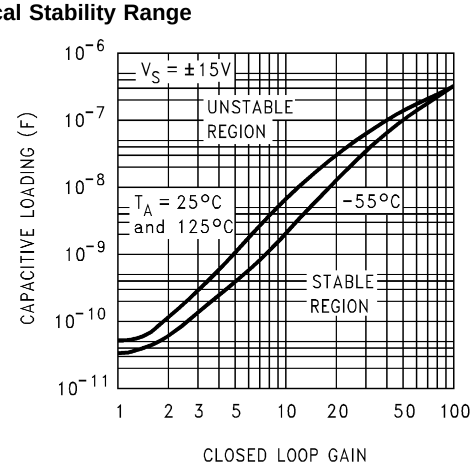

DS010254-40

### Follower Settling Time




DS010254-41

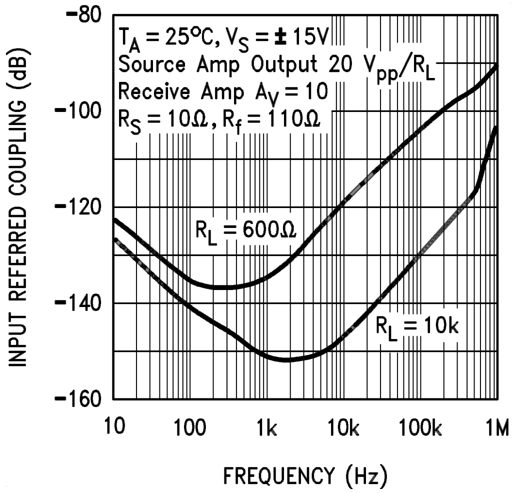
### Typical Stability Range




DS010254-42

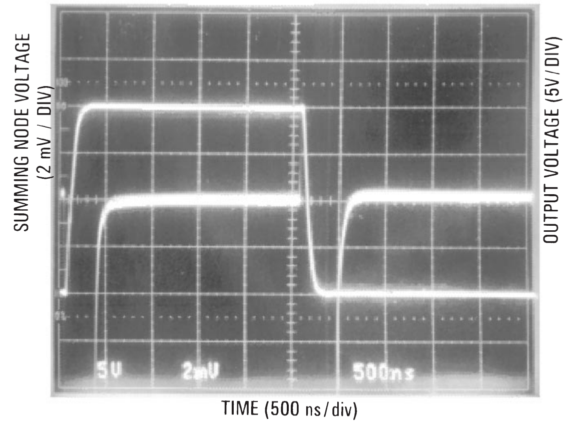
## Typical Performance Characteristics (Continued)

**Amplifier to Amplifier Coupling**



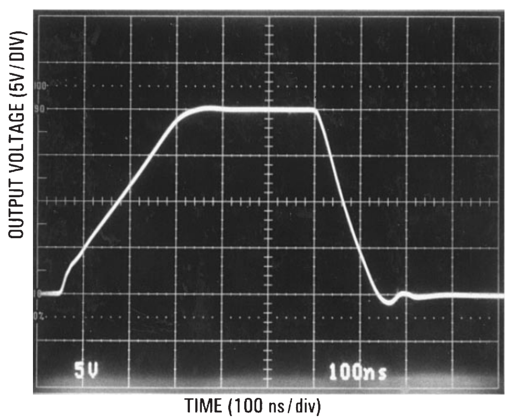

DS010254-23

**Settling Time, Vs = ±15V**



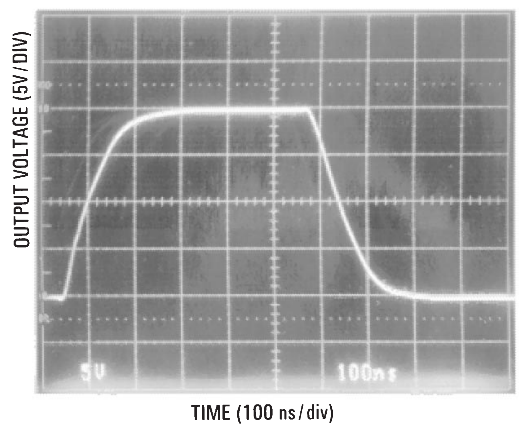

DS010254-7

**Step Response, Av = +1, Vs = ±15V**




DS010254-8

**Step Response, Av = −1, Vs = ±15V**




DS010254-9

## Application Information

### General

The LM6118/LM6218 are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

### Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 µF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

### Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

### Amplifier Shut Down

If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V− pin. This will reduce the power supply current by approximately 25%.

### Capacitive Loading

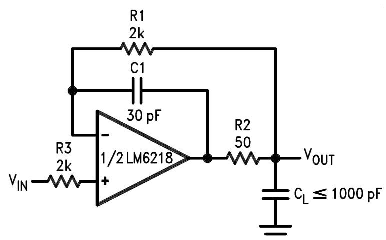
Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with

## Application Information (Continued)

50Ω. Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

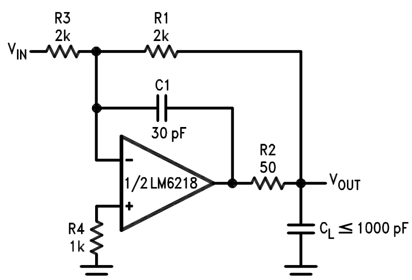
**Voltage Follower**




DS010254-10

For $C_L$ = 1000 pF, Small signal BW = 5 MHz
20 $V_{p-p}$ BW = 500 kHz

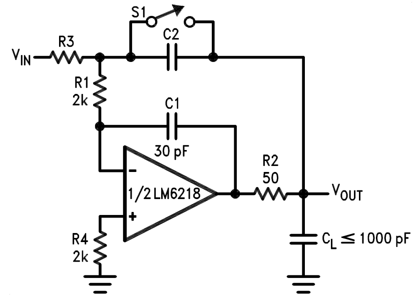
**Inverter**




DS010254-11

Settling time to 0.01%, 10V Step
For $C_L$ = 1000 pF, settling time ≈ 1500 ns
For $C_L$ = 300 pF, settling time ≈ 500 ns

**Integrator**




DS010254-12

Examples of unity gain connections for a voltage follower, Inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

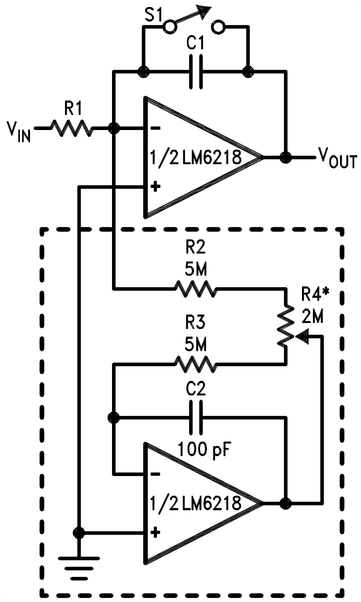
### Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

## Application Information (Continued)

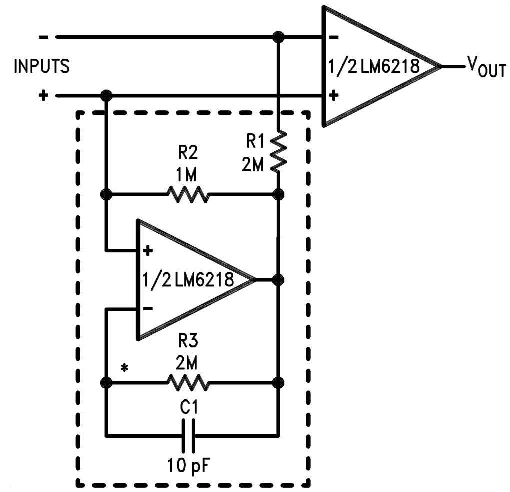
### Bias Current Compensation




DS010254-13

*adjust for zero integrator drift

**(a) Inverting Input Bias Compensation for Integrator Application**

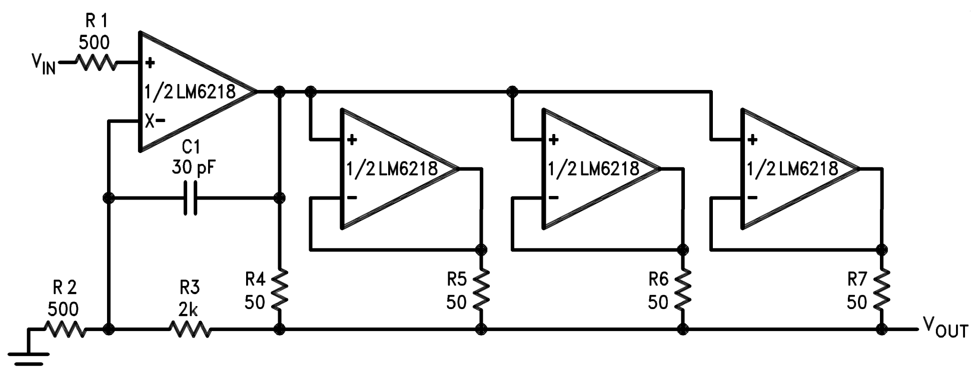



DS010254-14

*mount resistor close to input pin to minimize stray capacitance

**(b) Compensation to Both Inputs**

### Amplifier/Parallel Buffer

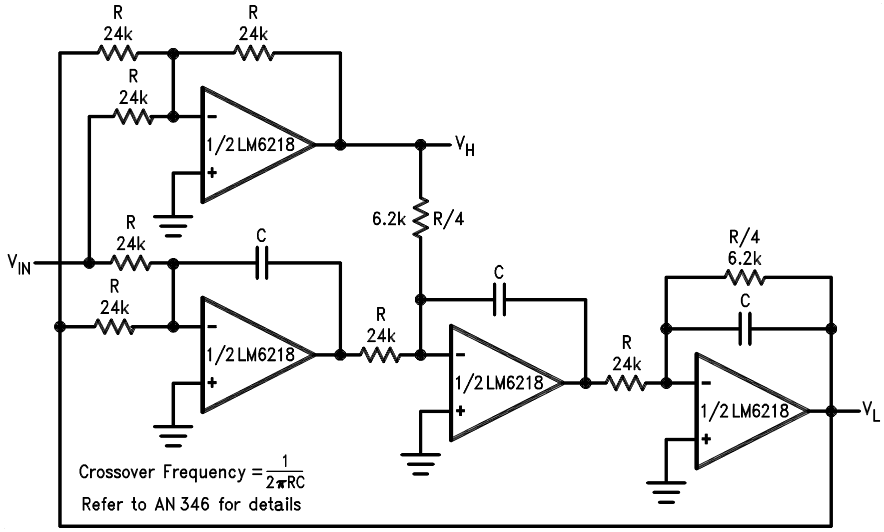



DS010254-15

$A_V = +5$, $I_{OUT} \le 80$ mA
$V_S = \pm 15V$, $C_L \le 0.01\ \mu F$
Large and small signal B.W. = 1.3 MHz (THD = 3%)

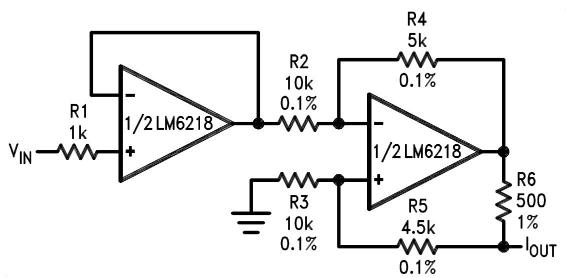
## Application Information (Continued)

### Constant-Voltage Crossover Network With 12 dB/Octave Slope




DS010254-16

### Bilateral Current Source




DS010254-17

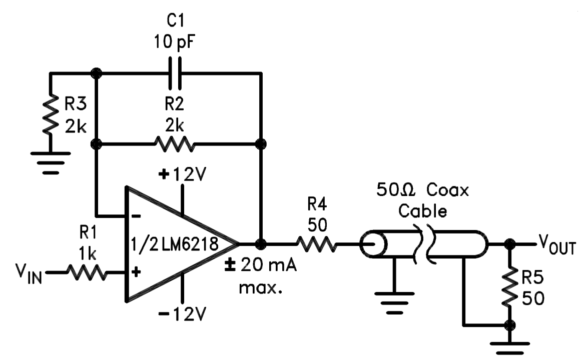
$V_S = \pm 15V$, $-10 \le V_{IN} \le 10V$

$$\frac{I_{OUT}}{V_{IN}} = \frac{R4}{R2\ R6} = \frac{1\ mA}{1V}$$

Output dynamic range = 10V − R6 $|I_{OUT}|$
$R_L = 500\Omega$, small signal BW = 6 MHz
Large signal response = 800 kHz

$$C_{out}\ \text{equiv.} = \frac{R2 + R4}{2\pi\ f_O\ R2\ R6} = 32\ pF\ (f_O = 15\ MHz)$$

### Coaxial Cable Driver

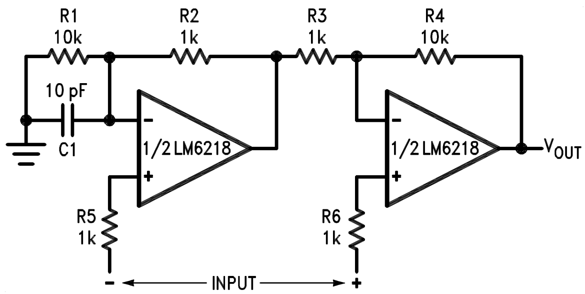



DS010254-19

Small signal (200 $mV_{p\text{-}p}$) BW ≈ 5 MHz

# Application Information (Continued)

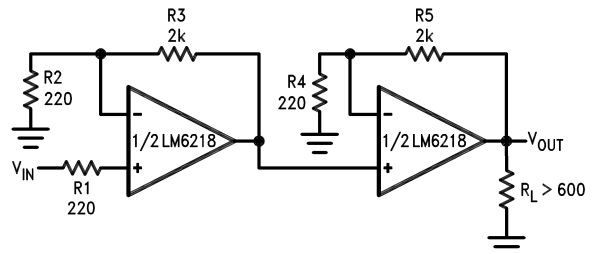
### Instrumentation Amplifier




DS010254-18

$A_V = 10$, $V_S = \pm 15V$, All resistors 0.01%
Small signal and large signal (20 $V_{P-P}$) B.W. ≈ 800 kHz

### 150 MHz Gain-Bandwidth Amplifier

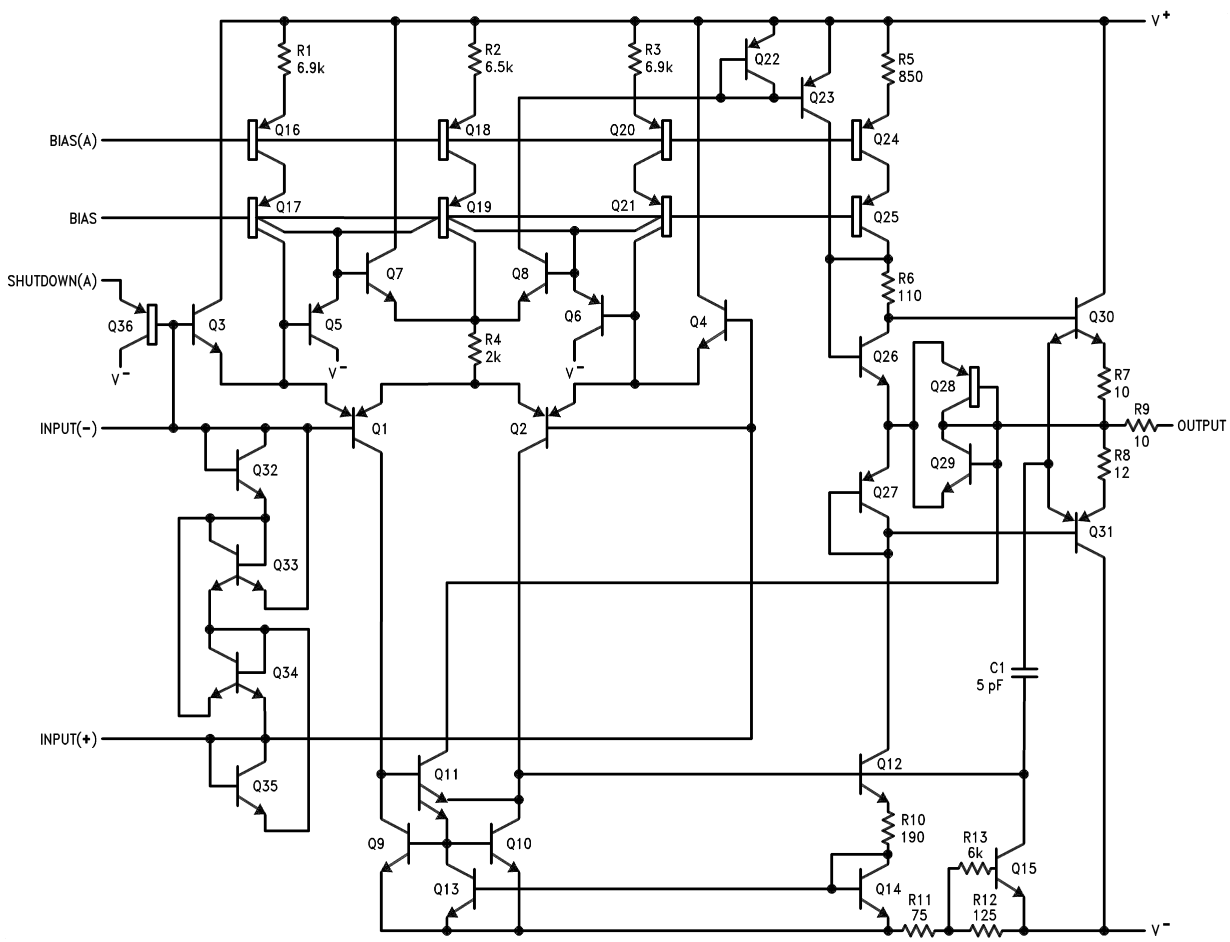



DS010254-20

$A_V = 100$, $V_S = \pm 15V$,
Small signal BW ≈ 1.5 MHz
Large signal BW (20 $V_{p-p}$) ≈ 800 kHz

# Schematic Diagram

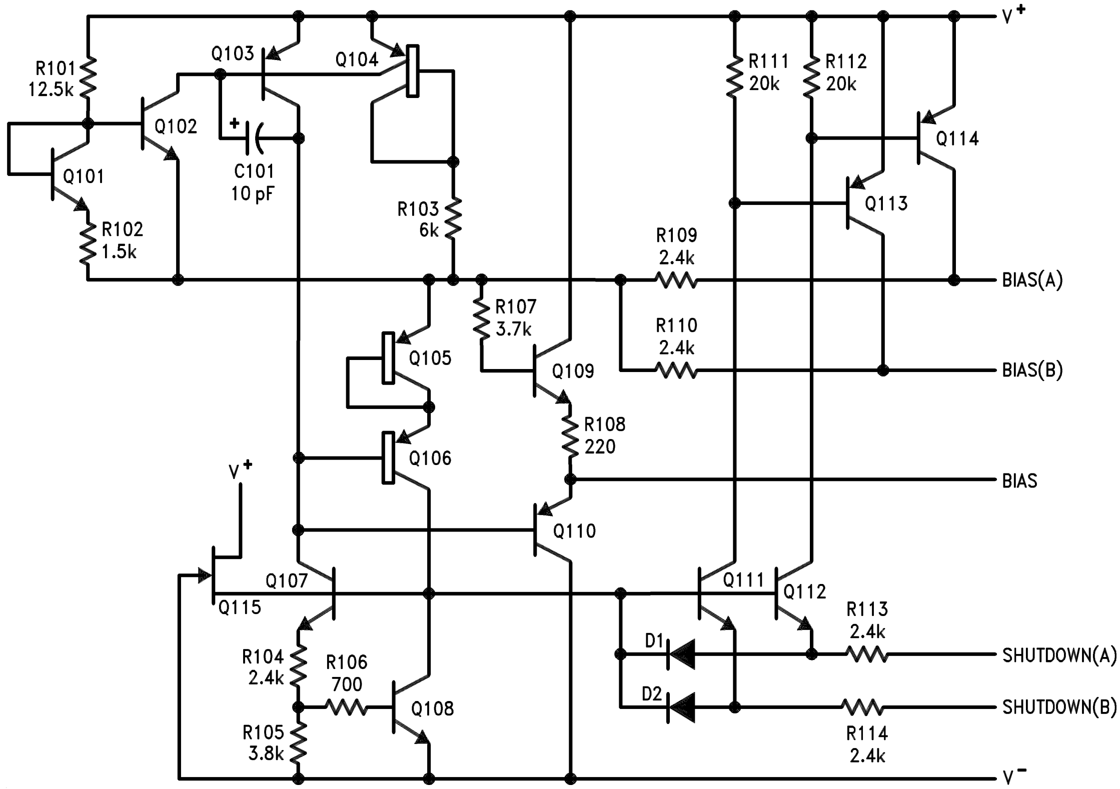
### 1/2 LM6118 (Op Amp A)




DS010254-21

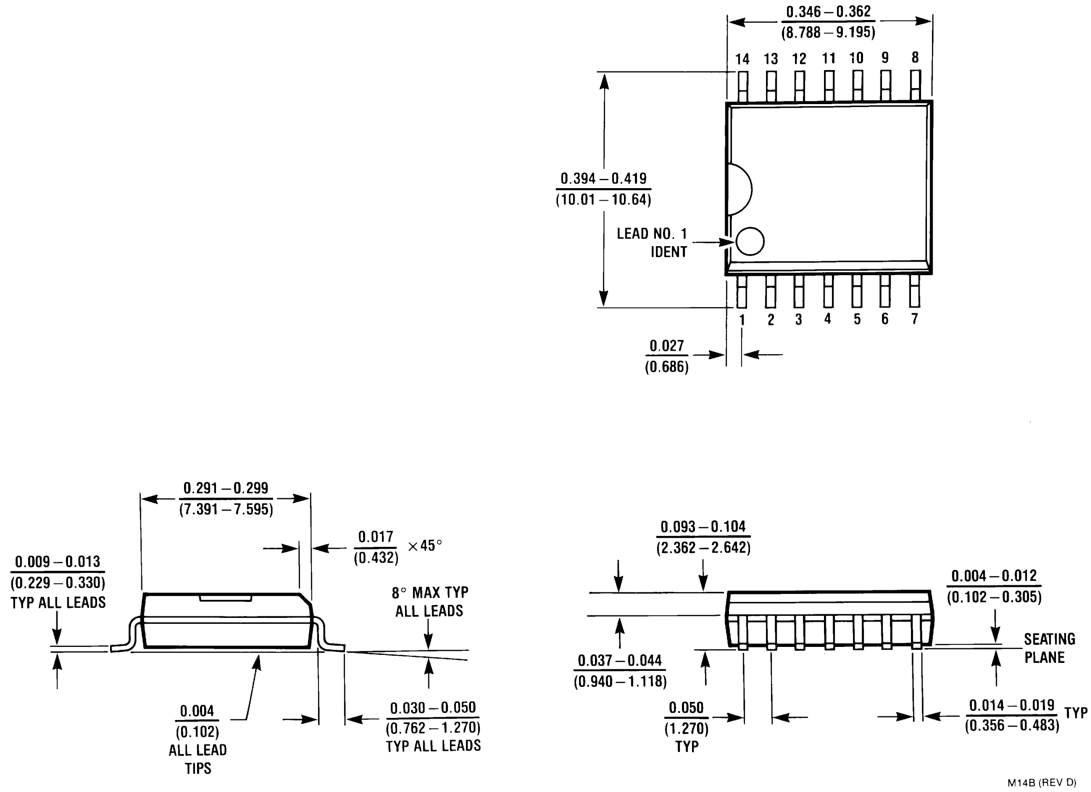
## Schematic Diagram (Continued)

**Bias Circuit**

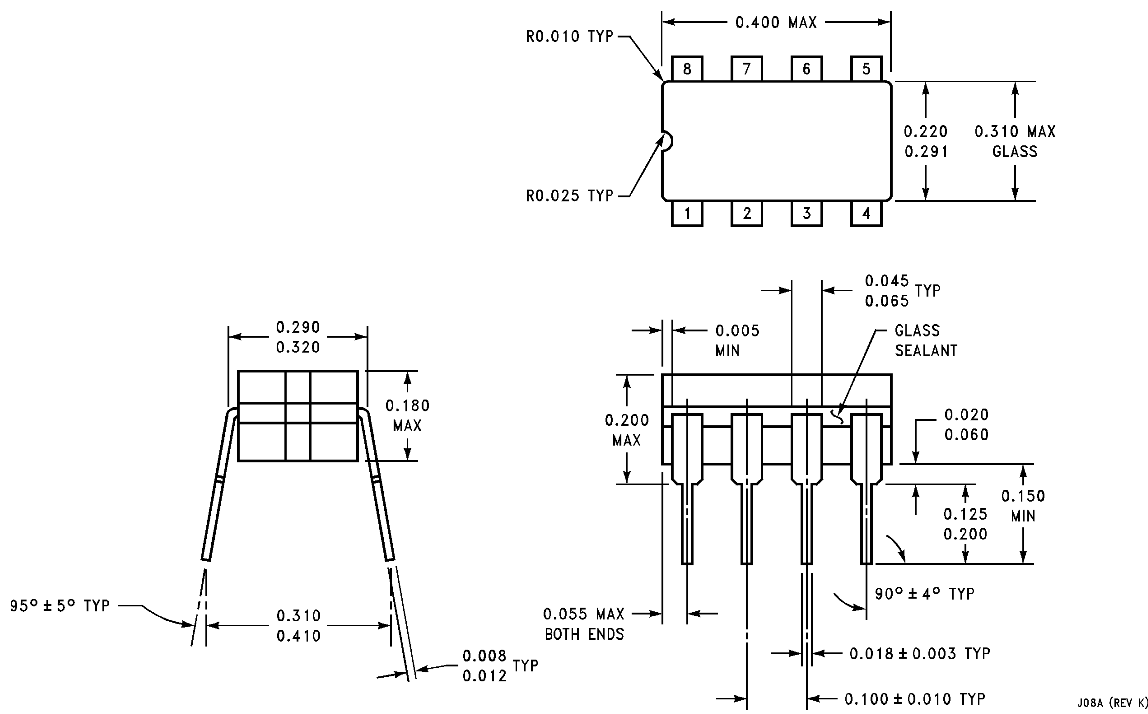



DS010254-22

## Physical Dimensions inches (millimeters) unless otherwise noted

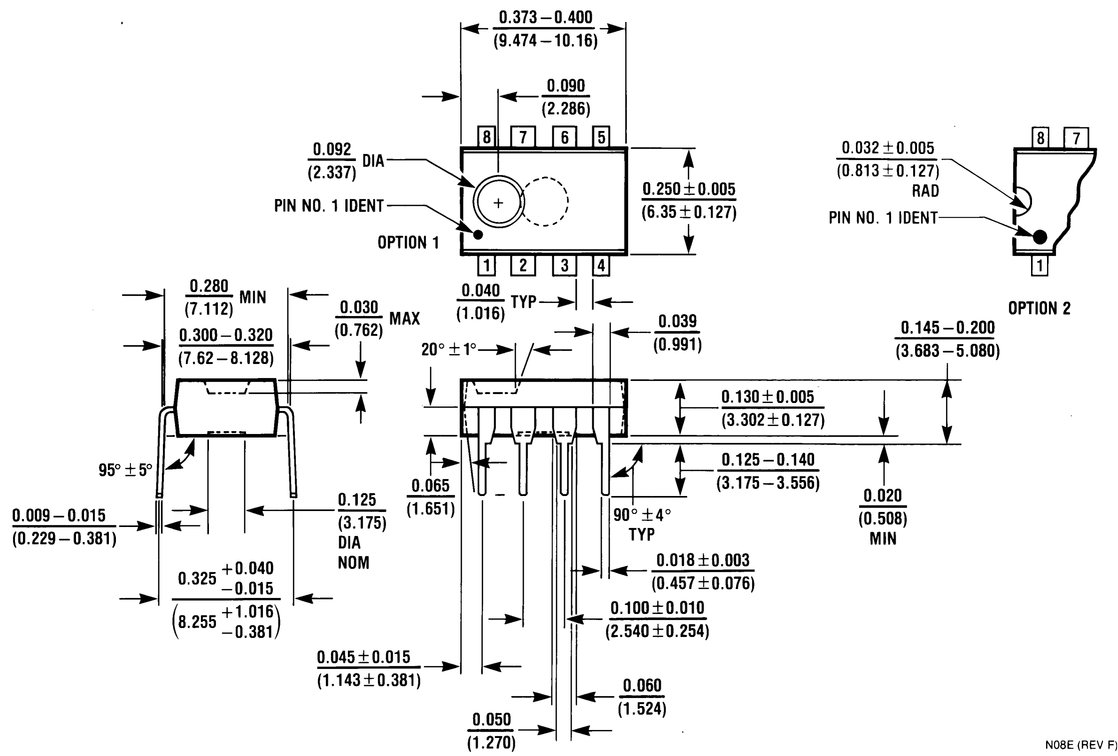



**8-Lead Molded Small Outline Package (M)**
**Order Number LM6218WM or LM6218WMX**
**NS Package Number M14B**




**8-Lead Molded Small Outline Package (M)**
**NS Package Number J08A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**8-Lead Molded Dual-In-Line Package (N)**
**Order Number LM6218N**
**NS Package Number N08E**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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